EECS 105 Project, Fall 2004

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Lab section	14
Lab time	W 12 – 3 pm
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Performance summary:

	specification	analysis	SPICE	difference [%]
Low frequency gain, a_{v0}	• 1000	6.31E+03	6.26E+03	0.886
Unity gain frequency, f_u (Hz)	• 50 MHz	5.50E+07	5.27E+07	4.26
Vo, min (V)	• 2V	2	1.9648	1.76
Vo, max (V)	• V_{DD} • 300 mV	4.7	4.7201	0.428
Power dissipation (W)	minimum	3.40E-02	3.40E-02	0.00

Scores:

Page	Max score	Actual score
Cover	5	
1	10	
2	10	
3	10	
4	5	
5-7	25	
8	5	
9	5	
10	5	
11	5	
12	5	
13	5	
14+	5	
Total	100	

Design Consideration in the choice of Topology

This design features a Common Source (CS) Stage cascaded with a Common Drain (CD) Stage. The CS Stage is designed to give the greater than 1000 gain, and since the gain must be greater than 1000, a NMOS cascode CS stage is used instead of a single CS stage. The result turns out the gain of the cascode CS stage is significantly higher than 1000 (at around 6000).

However, the gain of the CS stage depends heavily on the high output resistance of the CS stage, and the specs requires the circuit to drive a load of 10k ohm (RL). The low resistance RL parallel with Rout of the CS (RL//Rout_cs) causes the output resistance to be very small, which in turn causes the gain of the CS stage to drop significantly. In order to solve this problem, a CD stage is used to provide the high output resistance needed for the gain. This is done by connecting the input of the CD stage to the output of the CS stage.

For the Common Drain stage, in order to be in saturation, Vgs has to be greater than Vt. If NMOS is used, in order to have the NMOS stays in saturation

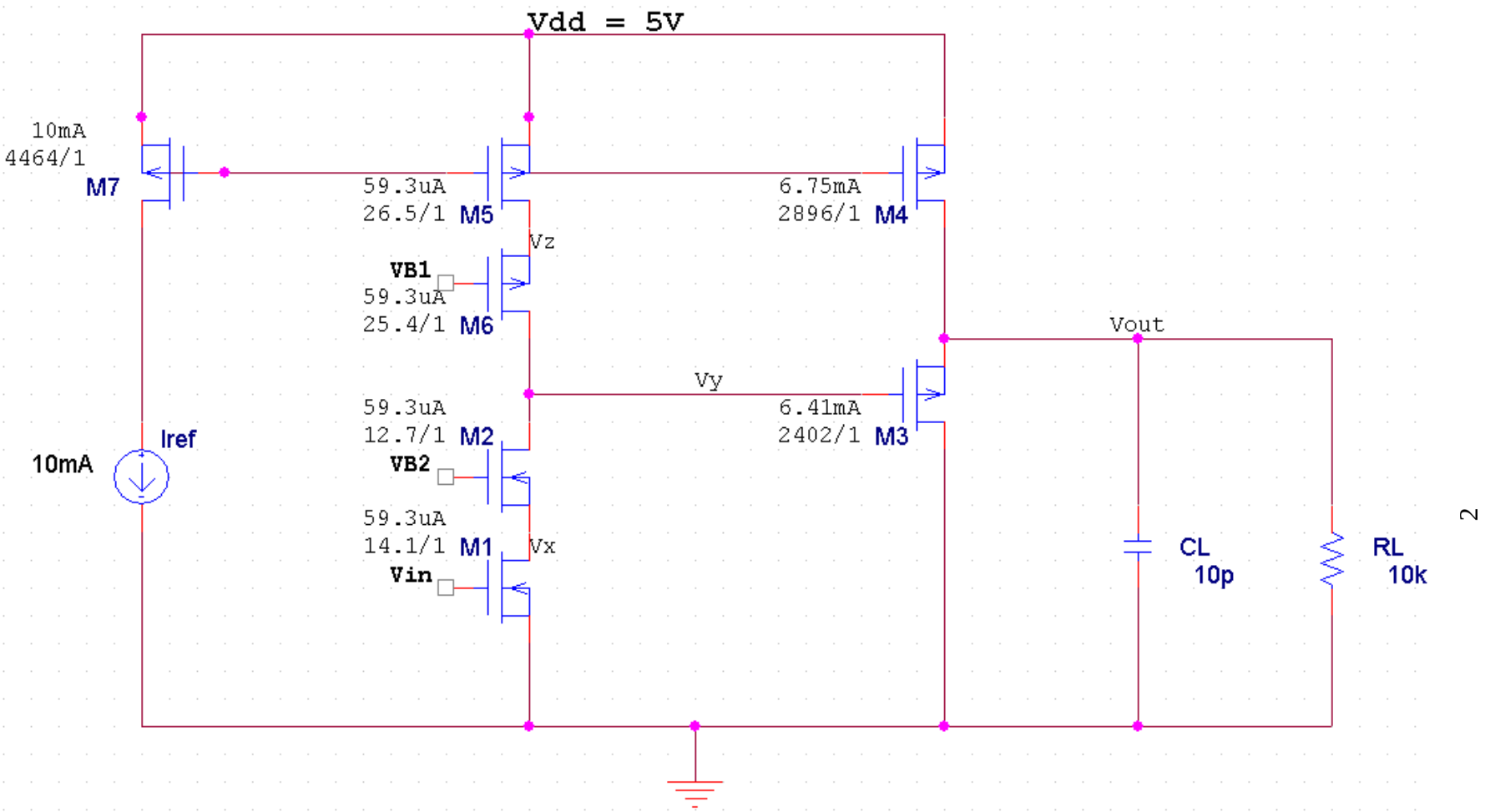
Vgs > Vtn
Vy – Vout > Vtn
Vy > Vtn + Vout
Vy > 1V + Vout, and if Vout = 4.7V
Vy > 5.7V, which is bigger than Vdd.

This means NMOS cannot be used to construct the common drain stage. In this case, PMOS is used instead.

Vdsat is chosen to be 200mV for all transistors. The value of Vdsat is proportional to Id, for which is then proportional to power. A smaller Vdsat value should requires less power to drive the transistor.

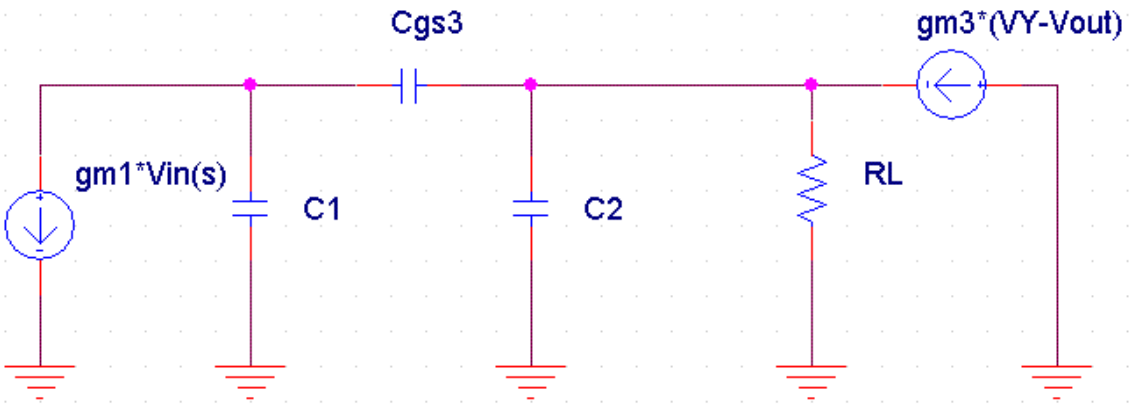
A NMOS cascode common source stage is used, so the current mirror is designed to use PMOS. In the common source stage, a cascode current source (CS + CG stage) is used instead of a single current mirror. This is because of a similar reason why I chose to use a CD stage, and that is the single stage CS amplifier has a relatively small resistance (ro) at Node y, whereas the resistance at Node y with a cascode CS is greater ($ro5 + ro6 + gm6 \cdot ro5 \cdot ro6$). The high output resistance at the output of the cascode CS stage contributes to the high gain ($Gm \cdot Rout$)of the cascode CS stage.

Schematic



VB1 = 2.6V dc source
VB2 = 1.7V dc source
Vin DC Bias = 1.2V

Small Signal Model



RL = 10K
C1 = Cgd2 + Cgd3 + Cgs3_eff + Cgd6
C2 = Cdb3 + CL + Cgd4 + Cdb4
gm1*Vin(s) = Two Port Model of the common source stage
Cgs3_eff = Cgs3 x (1- $gm1 \cdot (gm6 \cdot ro5 \cdot ro6 \,//\, gm2 \cdot ro1 \cdot ro2)$)

Cgs = $\frac{2}{3} \cdot W \cdot L \cdot Cox + W \cdot Col$

Cgd = $W \cdot Col$

Cdb =Cbs= $\frac{Cjo \cdot W \cdot Ldiff}{\sqrt{1+\frac{Vrev}{phiBp}}} + \frac{Cjswn \cdot (W + 2 \cdot Ldiff)}{\sqrt{1+\frac{Vrev}{phiBp}}}$ for PMOS

Analysis and Design of Output Range

Given the large signal circuit on page 2, Vout,min is chosen to be 2V, and Vout,max is chosen to be 4.7V. The operation point is Vo =1/2 (Vo, min +Vo, max) =3.35V.

The Vout range sets the voltage biases of the circuit. More specifically, Vout range sets the VB1, VB2, and Vin DC bias. The values of VB1, VB2, and Vin DC bias is to make sure all of the transistors in the circuit stay in the saturation region during operation range (2V-4.7V). Vout,max determines VB1, Vout,min determines VB2, and Vdsat determines Vin DC bias.

1. First consider VB1 when Vout,max equals 4.7V. Vy will be 3.5V. In order to have M6 stays in saturation, the following conditions have to be met.

Vsg – |Vtp| < Vsd	Vsg > |Vtp|
Vz – VB1 – 1V < Vz – Vy	Vz – VB1 > 1V
VB1 > Vy -1V	VB1 + 1.2V –VB1 > 1V
VB1 > 2.5V	1.2V > 1V

So I picked VB1 = 2.6V

2. Next is designing VB2, when Vout,min equals 2V. Vy will be 0.8V. In order to have M6 stays in saturation, the following conditions have to be met.

Vgs –Vtn < Vds	Vgs > Vtn
VB2 – Vx – 1V < Vy – Vx	VB2 – Vx > 1V
VB2– 1V < Vy	VB2 - (VB2 -1.2V) > 1V
VB2 <1.8V	1.2V > 1V

So I picked VB2 = 1.7V

3. For Vin DC bias, Vin,bias = Vdsat + Vtn = 1.2V. This is the input DC bias point.

Calculate Devices Parameters from Specs

1. Analysis and design low-frequency gain $av0$

In order to achieve low-frequency gain more than 1000, a cascade common source stage is chosen. However, the circuit is designed to drive a load resistance of 10k ohm, and the load resistance will lower the gain of the common source stage because of the low output resistance of the common source stage.

Due to the low output resistance of the common source (CS) stage, a common drain (CD) stage is placed between the common source stage and the load (RL).

$$gm = \frac{2 \cdot Id}{Vdsat}$$

$$ro = \frac{(1 + \lambda Vsd)}{\lambda \cdot Id} \text{ for PMOS}$$

The low-frequency gain ($av0$)
= Gain of the Common Source Stage x Gain of the Common Drain Stage

$$= gm1 \cdot (gm6 \cdot ro5 \cdot ro6 \,//\, gm2 \cdot ro1 \cdot ro2) \times gm3 \cdot (ro3 \,//\, ro4 \,//\, \frac{1}{gm3} \,//\, R_L)$$

=6.3119E+03

The gain of the circuit is well over 1000 with a CS stage and a CD stage. Basically, the gain meets the specs, and the next step is to make sure the unity frequency (*fu)* and second pole frequency (*fp2*) meets the specs.

2. Analysis and design of *fu* and poles

The specs requires the unity frequency (*fu)* to be greater than 50MHz. To leave a 10% safety margin, I picked the *fu* to be 55MHz. For the second pole *(fp2)*, the value of *fp2* must be greater than *fu*. I picked 1.5 x 50MHz, which is 75 MHz. The reason for choosing 75MHz is because usually if the circuit has feedback, it is usually a good idea to put the second pole at about 1.5 times the *fu*. Even this circuit does not involve feedback, I still choose *fp2* to be 75MHz. The higher the pole is, the more power the circuit requires. This is why I did not pick poles at extremely high values.

First of all I design the common drain stage. I chose the Output Node to be the second pole. By doing KCL on Node y and the Output Node (see page 3), equation 1 can be derived.

$$vo = -is \cdot \frac{1 + s\frac{Cgs3}{gm3}}{s\left(\left(1 + \frac{1}{gm3 \cdot RL}\right)C1 + \frac{1}{gm3 \cdot RL}Cgs3\right)\left(1 + s\frac{C2 + Cgs3 + \frac{Cgs3 \cdot C2}{C1}}{C1}\right)} \quad \ldots(1)$$

, where

C1 = Cgd2 + Cgd3 + Cgs3_eff + Cgd6

C2 = Cdb3 + CL + Cgd4 + Cdb4

Cgs3_eff = Cgs3 x (1- $gm1 \cdot (gm6 \cdot ro5 \cdot ro6 // gm2 \cdot ro1 \cdot ro2)$)

Cgs = $\frac{2}{3} \cdot W \cdot L \cdot Cox + W \cdot Col$

Cgd = $W \cdot Col$

Cdb =Cbs= $\frac{Cjo \cdot W \cdot Ldiff}{\sqrt{1+\frac{Vrev}{phiBp}}} + \frac{Cjswn \cdot (W + 2 \cdot Ldiff)}{\sqrt{1+\frac{Vrev}{phiBp}}}$ for PMOS

From equation (1),

$wz1 = -\frac{gm3}{Cgs3}$ = -1.1085E+09Hz

$wp1 = 0$

The equation (1) shows pole 1 is at zero rad/sec, but that is not true. This is because the drain of M2 is neglected for analysis. The correct value for wp1 can be calculated from equation 4.

The W3 of the common drain transistor M3 can be determined from the second pole by the equation (2).

$$wp2 = -\frac{gm3\left(1+\frac{1}{gm3 \cdot RL}\left(1+\frac{Cgs3}{C1}\right)\right)}{C2 + Cgs3 + \frac{Cgs3 \cdot C2}{C1}} \ldots(2)$$

First assume Cgd2, Cgd6, Cgd4 and Cdb4 to be zero. These neglected parasitic capacitors will be included later. Then all the terms in equation (2) can be express in terms of W3. With the calculated W3, current Id through M3 and M4 can be calculated. Thus, the widths of M3 and M4, as well as the parasitic capacitors of M3 and M4 can be calculated.

With W3, I go ahead and design the dimensions of the transistors of the common source stage. Node y is chosen to be the dominant pole (wp1), and the wp1 is related to the wu by equation 2.

$$wu = |avo| \, wp1 \cdot \sqrt{\frac{1}{1+\left(\frac{wu}{wp2}\right)^2}} \ldots(3)$$

On the other hand, wp1 is expressed in equation (4),

$$wp1 = -\frac{1}{(ro1 + ro2 + gm2 \cdot ro1 \cdot ro2)(C1 + \frac{Cgs3}{gm3 \cdot RL}} \approx -\frac{gm1}{|avo|\left(C1 + \frac{Cgs3}{gm3 \cdot RL}\right)} \ldots(4)$$

wp1 = - 6.6688E+04 rad/s

|fp1| = 1.0614E+04 Hz

Combining equation (3) and equation (4), equation (5) is formed to determine W1.

$$|wu| = \frac{gm1}{C1 + \frac{Cgs3}{gm3 \cdot RL}} \cdot \frac{1}{\sqrt{1 + \left(\frac{wu}{wp2}\right)^2}} \ldots(5)$$

With the W3 determined earlier, gm1 can be calculated. With gm1, the current Id through M1, M2, M5, and M6 can be calculated by equation (6). In turns, the dimension of M1, M2, M5, and M6 can be calculated by equation (7).

$$Id = \frac{Vdsat}{2 \cdot gm} \ldots(7)$$

$$W = \frac{2 \cdot Id \cdot L}{Kp \cdot (Vdsat)^2 (1 + \lambda \cdot Vds)} \ldots(8)$$

With the widths of M1, M2, M5, and M6, the parasitic capacitances in equation (2) can be calculated and reintroduced those parasitic capacitances into the equation (2). The parasitic capacitances of the common sources stage and the common drain stage are interdependent. In other words, one has to calculate the widths for one stage, and change the value of the other stage according to the new value. By iterating the values back and forth between the CS and CD stages several times until the final values and dimensions of transistors converge. This process is done with an Excel Spread Sheet attached.

The final calculated device parameters are shown in the following table as well as in the large signal diagram on page 2.

Device	Width (μm)	Length(μm)
M1	1.4120E+01	1
M2	1.2727E+01	1
M3	2.4025E+03	1
M4	2.8969E+03	1
M5	2.6476E+01	1
M6	2.5453E+01	1
M7	4.4643E+03	1

Iref (Bias current) is picked at 10mA to make sure the frequency of zero associated with the Node between M7 and Iref is further away from fu (at least 1 decade away) in the frequency plot. Thus the zero would not affect the Bode Plot of the circuit.

Another list of device parameters can be found on page 9.

3. Power Dissipation $= Vdd \cdot (I_{ds4} + I_{ds5})$

$= 5V \cdot (6.75E-03A + 5.93E-05A)$

$= 34mW$

Operating point analysis for *Vo* =1/2 (*Vo*, min +*Vo*, max)

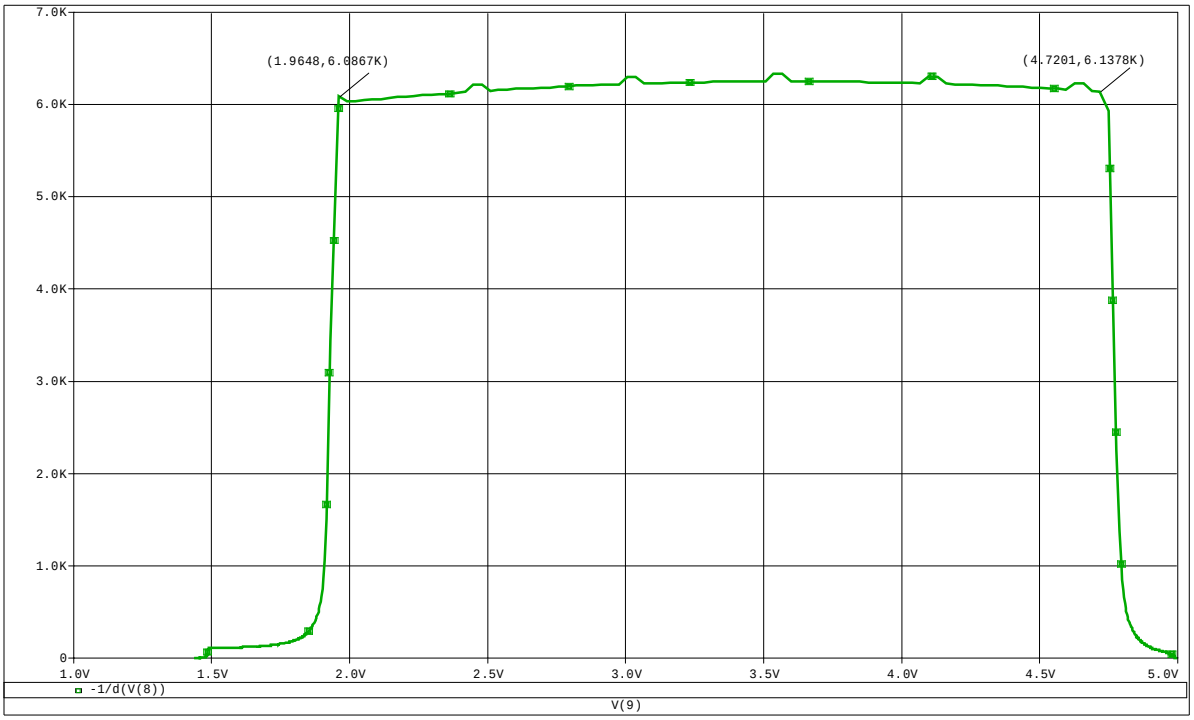
Device	*I D*	*gm*	*Vdsat*	*CGS*	*CGD*	*CBS*	*CBD*
M1 analysis	5.93E-05	5.93E-04	2.00E-01	5.41E-14	7.06E-15	3.00E-14	2.45E-14
SPICE	5.93E-05	5.93E-04	2.00E-01	5.42E-14	7.06E-15	3.00E-14	2.45E-14
difference [%]	1.18E-02	1.18E-02	0.00E+00	8.28E-02	2.12E-02	1.52E-01	1.31E-01
M2 analysis	5.93E-05	5.93E-04	2.00E-01	4.88E-14	6.36E-15	2.71E-14	1.67E-14
SPICE	5.93E-05	5.93E-04	2.00E-01	4.88E-14	6.36E-15	2.71E-14	1.67E-14
difference [%]	1.18E-02	1.18E-02	0.00E+00	3.14E-02	3.14E-02	7.53E-02	2.40E-01
M3 analysis	-6.41E-03	6.41E-02	-2.00E-01	9.21E-12	1.20E-12	5.04E-12	2.30E-12
SPICE	-6.41E-03	6.42E-02	-2.00E-01	9.21E-12	1.20E-12	5.04E-12	2.42E-12
difference [%]	5.15E-06	1.04E-01	0.00E+00	2.50E-02	8.33E-02	9.13E-02	4.96E+00
M4 analysis	-6.75E-03	6.75E-02	-2.00E-01	1.11E-11	1.45E-12	6.08E-12	3.74E-12
SPICE	-6.75E-03	6.75E-02	-2.00E-01	1.11E-11	1.45E-12	6.08E-12	3.74E-12
difference [%]	2.52E-06	2.52E-02	0.00E+00	6.77E-02	1.24E-01	4.33E-02	9.28E-02
M5 analysis	-5.93E-05	5.93E-04	-2.00E-01	1.01E-13	1.32E-14	5.60E-14	3.77E-14
SPICE	-5.93E-05	5.93E-04	-2.00E-01	1.02E-13	1.32E-14	5.60E-14	3.77E-14
difference [%]	1.18E-06	1.18E-02	0.00E+00	3.12E-02	2.65E-01	2.32E-02	1.23E-01
M6 analysis	-5.93E-05	5.93E-04	-2.00E-01	9.76E-14	1.27E-14	5.38E-14	3.31E-14
SPICE	-5.93E-05	5.93E-04	-2.00E-01	9.76E-14	1.27E-14	5.38E-14	3.31E-14
difference [%]	1.18E-06	1.18E-02	0.00E+00	5.05E-02	1.89E-01	7.58E-02	7.81E-02
M7 analysis	-1.00E-02	1.00E-01	-2.00E-01	1.71E-11	2.23E-12	9.38E-12	6.32E-12
SPICE	-1.00E-02	1.00E-01	-2.00E-01	1.71E-11	2.23E-12	9.38E-12	6.32E-12
difference [%]	0.00E+00	0.00E+00	0.00E+00	9.87E-02	9.42E-02	4.90E-02	1.41E-02

Power dissipation:
analysis 34mW TOTAL POWER DISSIPATION 8.40E-02 WATTS
SPICE 34mW Iref power = 10mA x 5V = 50mW

	analysis [Hz]	SPICE [Hz]	difference [%]
Pole 1 frequency, *f p*1	1.0614E+04	1.0528E+04	0.81025
Unity gain frequency, *f u*	5.5000E+07	5.2656E+07	4.2618
Pole 2 frequency, *f p*2	7.5000E+07	7.3560E+07	1.9200
Zero 1 frequency, *f z*1	1.1085E+09	1.0692E+09	0.035496

Verification of *av*0 vs. *Vo* over the output range

Avo vs Vout

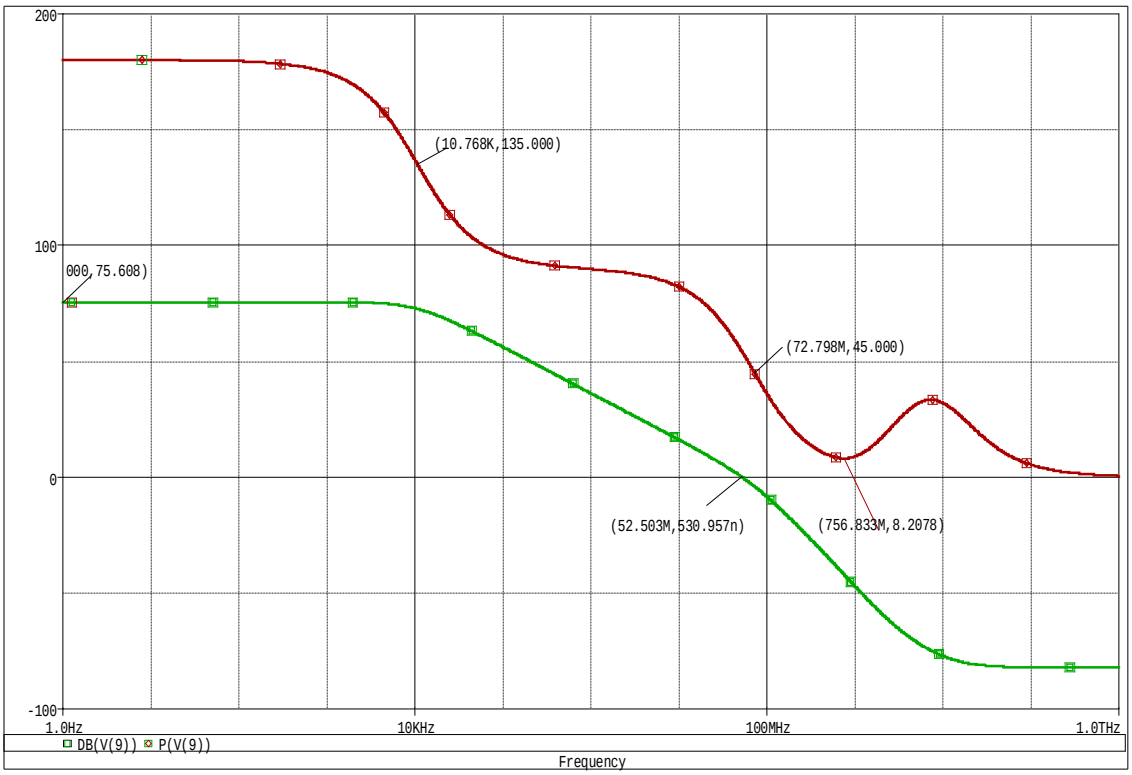


From the graph, we see that the output range is from 1.9648V to 4.7201V. Vout,min (1.9648V) is less than 2V, and Vout,max (4.7201V) is greater than 4.7V.

The Vout, min is less than 2V, and the Vout,max is greater than 4.7V. Therefore, I use the Spice values (1.9648V and 4.7201V) for my Vo,min and Vo,max analysis on page 10 and page 11.

I chose the output range to be the corners of the Avo vs Vout plot because the circuit is designed to work at around 6000 gain, instead that of 1000. (This is also an advice from Amin too use the corner instead of 1k).

Bode plot and poles for $V_o = V_{o,\min}$.



Frequency response for $V_o = V_{o,\min}$ = 1.9648V

Vin = 1.200180054V

Low frequency gain a_{vo} = 6.031 x 10^3

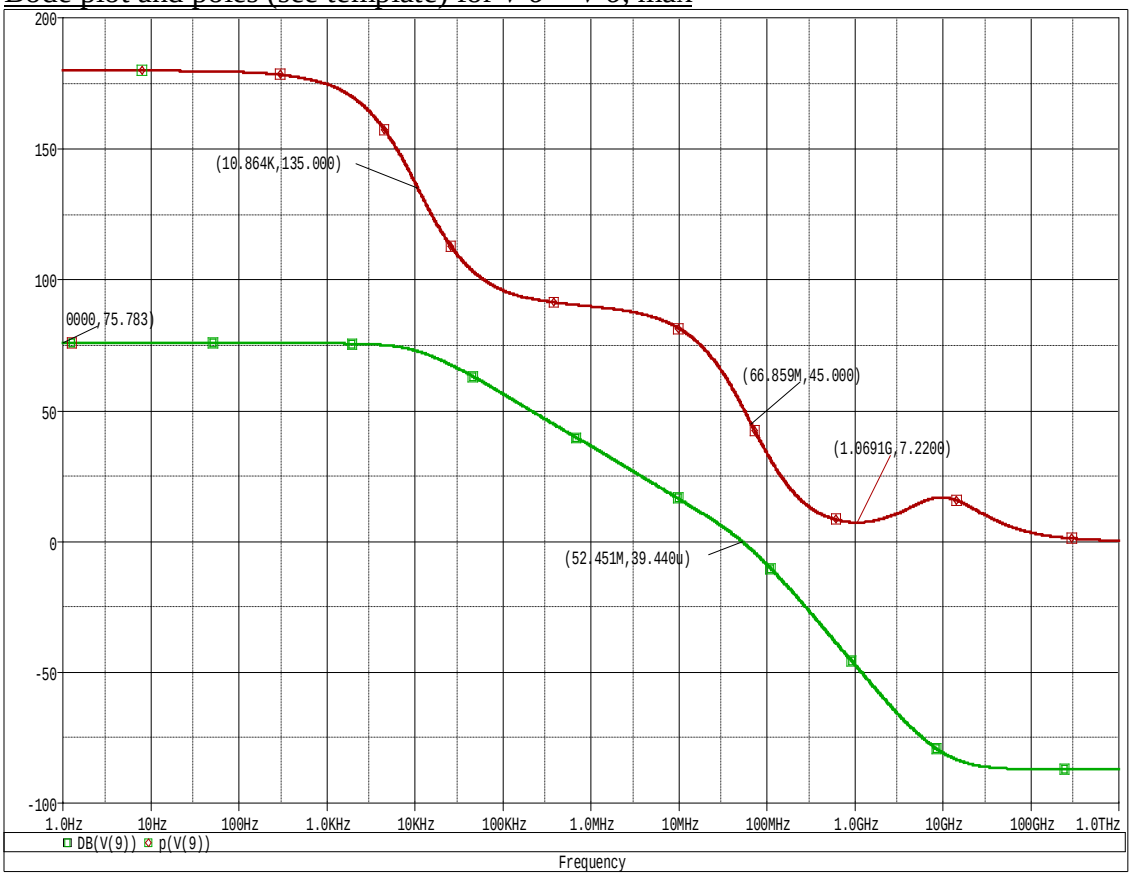
	analysis [Hz]	SPICE [Hz]	difference [%]
Pole 1 frequency, f_{p1}		1.0768E+04	
Unity gain frequency, f_u		5.2503E+07	
Pole 2 frequency, f_{p2}		7.2798E+07	
Zero 1 frequency, f_{z1}		7.5683E+08	

The hand analysis is not performed, because the circuit is not designed to operate at Vo,min. (This is also an advice from Chuwuba not to calculate analysis for this part)

f_{p2} = 72.8M > f_u = 52.5 M > 50M, so f_u and f_{p2} meet the specs at Vo,min.

a_{vo} = 6.031 x 10^3 > 1000, so a_{vo} meets the specs.

Bode plot and poles (see template) for $V_o = V_{o,max}$



Frequency response for $V = V_o$, max = 4.7201V

Vin = 1.199735045V

Low frequency gain $a_{vo} = 6.150 \times 10^3$

	analysis [Hz]	SPICE [Hz]	difference [%]
Pole 1 frequency, f_{p1}		1.0864E+04	
Unity gain frequency, f_u		5.2451E+07	
Pole 2 frequency, f_{p2}		6.6859E+07	
Zero 1 frequency, f_{z1}		1.0691E+09	

f_{p2} = 66.9M > f_u = 52.5 M > 50M, so f_u and f_{p2} meet the specs at Vo,max.
$a_{vo} = 6.150 \times 10^3 > 1000$, so a_{vo} meets the specs.
The hand analysis is not performed, because the circuit is not designed to operate at Vo,max. (This is also an advice from Chuwuba not to calculate analysis for this part)
Notice the frequency of the fp2 is further off from the designed 75MHz. This is because with high Vout, more current is drawn to the RL, less current go through M3, so gm3 is smaller, so wp2 is smaller.

Discrepancies > 5% between hand analysis and SPICE

(Empty)

Comments

1. The Disappearance of Cdb2

Notice Cdb2 was supposed to be included in C1 (see page 3), but instead, Cdb2 is neglected because of the feedback of transistor M2. The reason for neglecting Cdb2 is that when current (I_{Cdb2}) from Node Y (See page 3) is flowing through capacitor Cdb2, which is connected between the drain of M2 and the bulk of M2, the current (I_{Cdb2}) reaches Node X (See page 3) then problem occurs.

At Node X, the resistance "looking" up is 1/gm6, and the resistance "looking" down is $gm2 \cdot ro1 \cdot ro2$. The resistance "looking" down (20.6 Mohm) is much greater than the resistance "looking" up (1.69 kohm), so most of the current at Node X goes right back to Node Y. In this case, the capacitance "feels" like very small because of the feedback. In other words, the feedback due to the low impedance at the source of M2 makes Cdb2 negligible.

Similar situation also applies to Cdb6, which means the effective capacitance of Cdb6 is also close to zero. Cdb6 is also neglected in the circuit.

2. The Vo,min and Vo,max Range

The Vo,min and Vo,max range is not set at Gain=1k. Instead, they are set at Gain=6.1k. This is because the gain of the circuit is designed to work at 6.1k instead of 1k.

3. Monstrous Huge Transistor Size

Some of the transistors are in the dimension of several millimeters. For a real circuit, the size of the width should be in the order of micro or nano-scale. This large dimension is acceptable only because this is my first very circuit design, but the size of the transistor is certainly not practical in the real world. Such a huge transistor requires a lot of current, and is not power efficient.

4. Project in EE 105 Piggy Test

I was informed a project in EE 105 is a test. My comment to this test is, the project is generally fun, even I have spent 2 whole weekends (70 hours+) on the project. However, this is a general comment that we don't know enough to do the project when the project requirements first comes out.

Conclusions.

There were two main challenges in this project. The output range and the mathematical challenge to determine the width of all the transistors.

The output range limits the choice of topology at the output stage. More specifically, the high Vo,max prohibits the use of NMOS as the CD stage.

The second challenge is to find the formulas and know exactly what to iterate to get the interdependent widths for each transistor. The calculation procedure is certainly the most difficult part of the project.

Annotated SPICE Input with all Analysis Statements

Vout, min

```
****     SMALL-SIGNAL CHARACTERISTICS


    V(9)/Vin = -6.031E+03

    INPUT RESISTANCE AT Vin =  1.000E+20

    OUTPUT RESISTANCE AT V(9) =  1.508E+01
```

Vout, max

```
****     SMALL-SIGNAL CHARACTERISTICS


    V(9)/Vin = -6.150E+03

    INPUT RESISTANCE AT Vin =  1.000E+20

    OUTPUT RESISTANCE AT V(9) =  1.579E+01
```

Vout, Mid = 3.35V

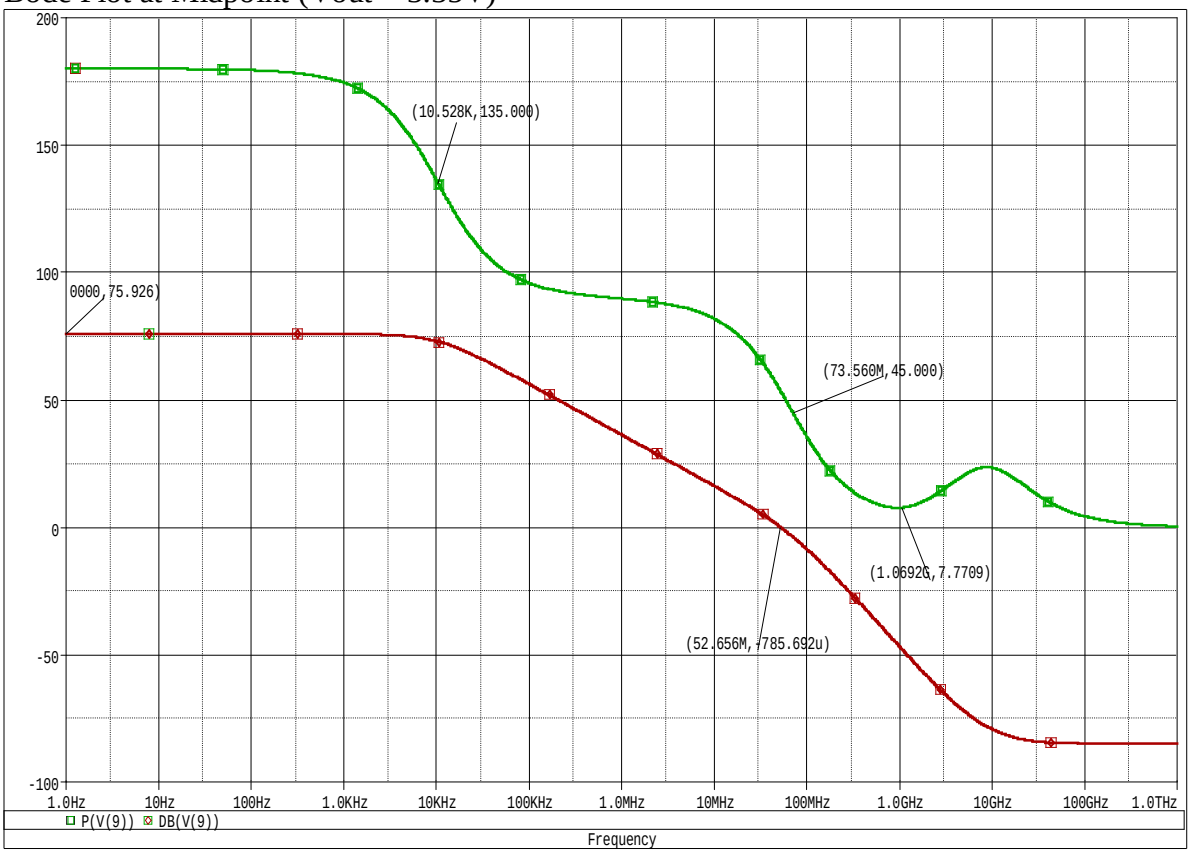
```
****     SMALL-SIGNAL CHARACTERISTICS


    V(9)/Vin = -6.256E+03

    INPUT RESISTANCE AT Vin =  1.000E+20

    OUTPUT RESISTANCE AT V(9) =  1.531E+01
```

Bode Plot at Midpoint (Vout = 3.35V)



	analysis [Hz]	SPICE [Hz]	difference [%]
Pole 1 frequency, *f p*1	1.0614E+04	1.0528E+04	0.81025
Unity gain frequency, *f u*	5.5000E+07	5.2656E+07	4.2618
Pole 2 frequency, *f p*2	7.5000E+07	7.3560E+07	1.9200
Zero 1 frequency, *f z*1	1.1085E+09	1.0692E+09	0.035496