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Borivoje Nikolic Homework #5: Delay EECS 141

Problem #1 Fanout and Buffer Delay - SPICE

From lecture 9, we have that:

$Tp=tp_0(1+f/\gamma)$

In this problem, we will look into the factor γ for a minimum sized inverter and relate it to the other parameters. Let Vdd=2.5v, and use the following for your simulations:

.lib '/home/ff/ee141/MODELS/g25.mod' TT

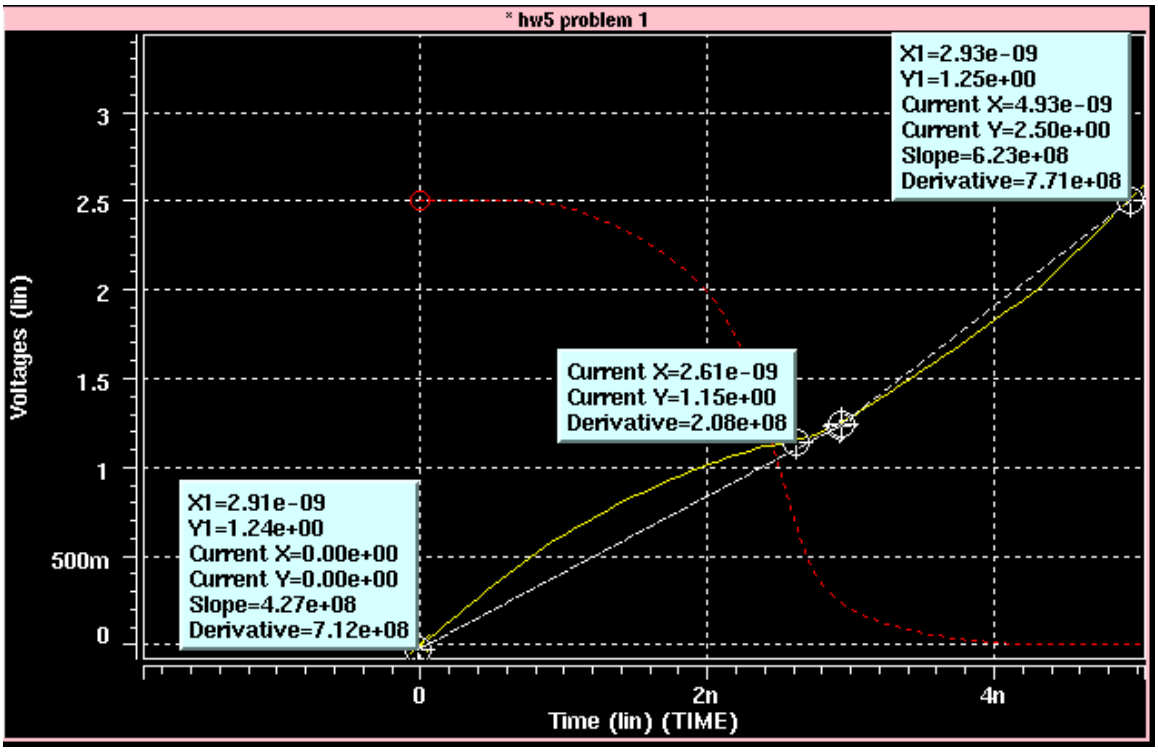
.subckt INV Vdd Gnd Vin Vout
M1 Vout Vin Vdd Vdd pmos l=0.24u w=0.6u
M2 Vout Vin Gnd Gnd nmos l=0.24u w=0.36u
.ends

a) Run a transient simulation for a single unloaded inverter with a 1uA current charging the input from 0 to 2.5v (you may have done this already in your solution for HW3). Estimate the input capacitance from the waveform at the input. Also, what is the worst case instantaneous input capacitance?

Hint: You can use Measure->Point in Awaves to see the slope of the input voltage when it's moving the most slowly

```
* hw5 problem 1
.option brief nomod post
.lib '/home/ff/ee141/MODELS/g25.mod' TT

.param vddp=2.5

VDD vdd 0 'vddp'

.subckt INV Vdd Gnd Vin Vout
M1 Vout Vin Vdd Vdd pmos l=0.24u w=0.6u
M2 Vout Vin Gnd Gnd nmos l=0.24u w=0.36u
.ends


Xinv1 vdd   0     v1    v2    INV


* PART a: extract input cap
IIN 0 v1 1u
```

```
.ic v(v1)=0
.meas t1 trig v(v1) val=0.0001 cross=1 targ v(v1) val='vddp/2' cross=1
.meas t2 trig v(v1) val='vddp/2' cross=1 targ v(v1) val='vddp' cross=1
.tran 0.01ns 10ns

.end
```



The capacitance going from 0 to 1.25v is C=1uA/(0.427V/ns) = 2.3fF
From 1.25 to 2.5v, C= 1uA/(0.623V/ns) = 1.6fF
The average for these transitions is: (2.3+1.6)/2 = 1.97fF. Just taking the slope from 0 to 1.25V would also give the same result.

The worst case instantaneous capacitance is 1uA/(0.208V/ns) = 4.8fF

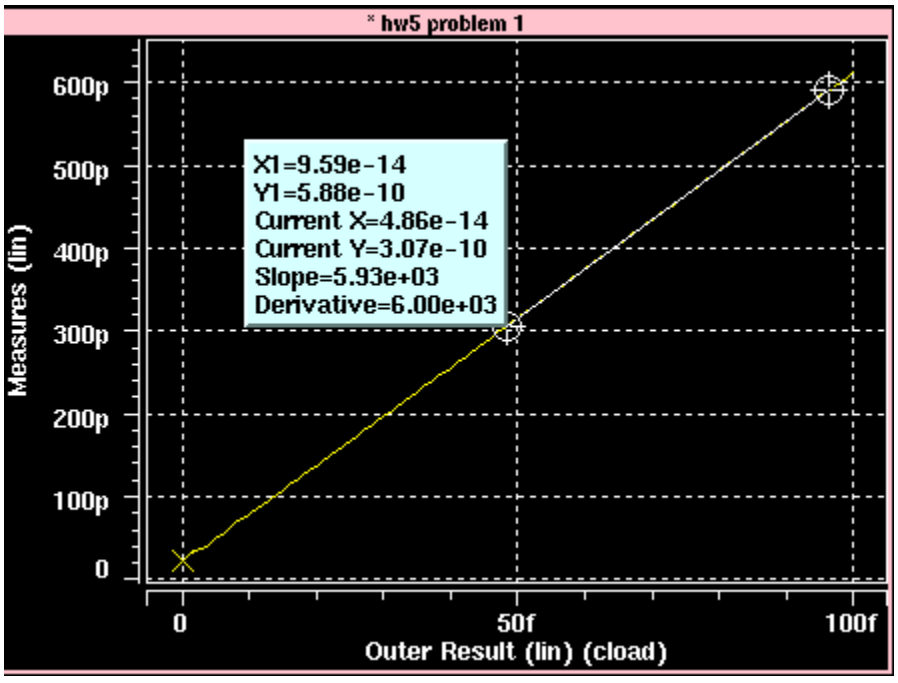
This worst-case is significantly larger as it comes when the NMOS transistor is on the edge of triode region where there is a significant gate-channel capacitance experiencing the miller effect, and the gain of the inverter is still large. The same effect isn't as apparent (but still exists) for PMOS because they have less gain.

b) Measure the propagation delay for a sharp rising edge going through a single inverter driving loads of 0 through 100fF. Extrapolate an estimate of the intrinsic output capacitance.

```
* hw5 problem 1
```

The question asks for 0 to 100fF loads, but we'll just show 0 to 20 here. The rest of the delay/capacitance curve is a continuation of the straight line we see here and is not interesting aside from noting that the straight line trend does continue.

```
.option brief nomod post
.lib '/home/ff/ee141/MODELS/g25.mod' TT

.param vddp=2.5

VDD vdd 0 'vddp'

.subckt INV Vdd Gnd Vin Vout
M1 Vout Vin Vdd Vdd pmos l=0.24u w=0.6u
M2 Vout Vin Gnd Gnd nmos l=0.24u w=0.36u
.ends

.param cload=0f

Xinv1 vdd   0     v1    v2    INV
C2    v2    0     'cload'

Vin   v1    0     dc    0     pulse(0 'vddp' 1p 1p 10n)


* part b: - extrapolate intrinsic output cap
.meas tfall trig v(v1) val='vddp/2' cross=1  targ v(v2) val='vddp/2'
cross=1
.tran 0.01ns '1ns' sweep cload 0f 20f 1f

.end
```



The curve has a bit of a wiggle for small loads (<5fF or so), but smooths out for larger loads. We'll extrapolate from two points out where the curve is straighter.

C_{int} =(3.07e-10/6e3)-4.86e-14 = 2.57fF

It's acceptable to fit to other points on the curve, depending on what actual load capacitances you anticipate having to drive, and your extracted capacitance may be somewhat different. If you're ambitious, you could do a linear regression, but a two point extrapolation is adequate.

c) So far, we've run the inverter with fictitious inputs and loads. To better capture how it would behave in a real environment, simulate a geometrically tapered chain of 8 inverters with fanout factor f. Give a sharp rising edge at the input of the first inverter and a large capacitor loading the last. Use your estimate of input capacitance from part a) to scale this load to emulate a continuation of the inverter chain. Measure the propagation delay of an inverter in the middle of the chain, for fanouts of 1 through 5, and estimate γ from the results.

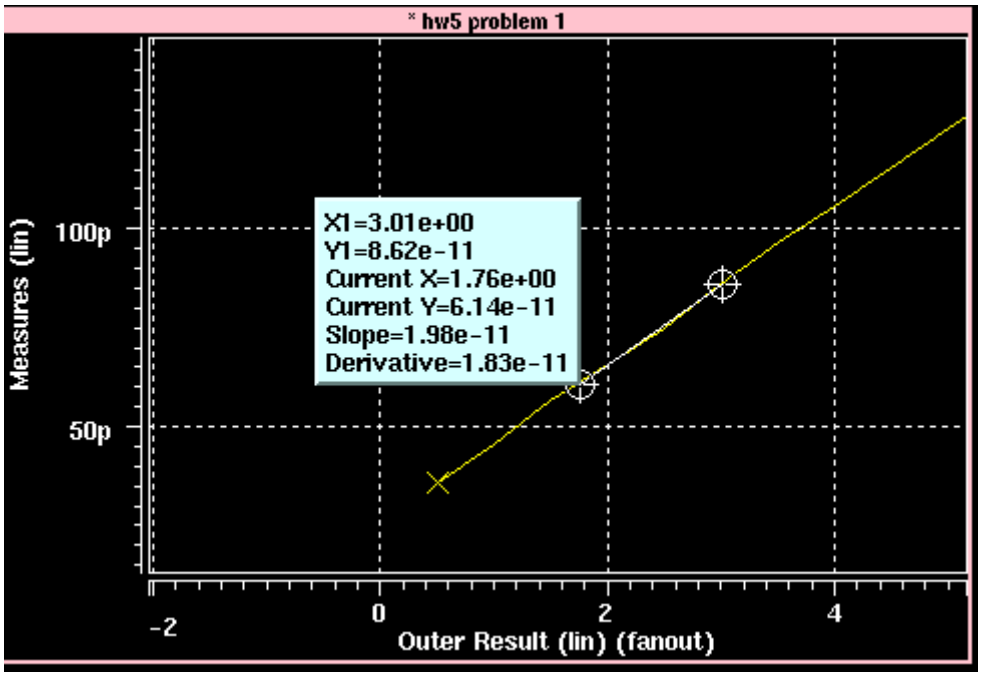
Tip: Rather than measuring the delay through a single inverter, measure across a consecutive pair of inverters, and take half of that delay. This will average out the differences between rising and falling edges, and also make the measurement independent of the switch level you use to trigger the delay measurement.

Tip: You can use a multiplier factor when instantiating an inverter in the chain, e.g.

```
.param f=3
….
Xinv2  vdd   0    v2   v3   INV   M='f'
Xinv3  vdd   0    v3   v4   INV   M='f**2'
```

```
* hw5 problem 1
.option brief nomod post
.lib '/home/ff/ee141/MODELS/g25.mod' TT

.param vddp=2.5

VDD vdd 0 'vddp'

.subckt INV Vdd Gnd Vin Vout
M1 Vout Vin Vdd Vdd pmos l=0.24u w=0.6u
M2 Vout Vin Gnd Gnd nmos l=0.24u w=0.36u
.ends

.param fanout=1
.param cin=1.97f

Vin   v1    0     dc    0     pulse(0 'vddp' 1p 1p 10n)
```

```
Xinv1 vdd    0      v1     v2     INV
Xinv2 vdd    0      v2     v3     INV    M='fanout'
Xinv3 vdd    0      v3     v4     INV    M='fanout**2'
Xinv4 vdd    0      v4     v5     INV    M='fanout**3'
Xinv5 vdd    0      v5     v6     INV    M='fanout**4'
Xinv6 vdd    0      v6     v7     INV    M='fanout**5'
Xinv7 vdd    0      v7     v8     INV    M='fanout**6'
Xinv8 vdd    0      v8     v9     INV    M='fanout**7'
C9    v9     0      'cin*fanout**8'


* part c: estimate gamma
.meas delay2 trig v(v5) val='vddp/2' cross=1 targ v(v7) val='vddp/2'
cross=1
.meas tran tp param='delay2/2'
.tran 0.01ns 'fanout*1ns' sweep  fanout 0.5 15 0.5

.end
```



Again, the exact value will vary with how you extrapolate. For the points chosen here, we get:

$\gamma = (6.14/1.98)-1.76 = 1.3$

d) In theory, what should the relationship be between your answers for parts a, b, and c? How do your results compare? Speculate on which values can be trusted and why the others may be questionable. Suggest other approaches for extracting the suspect parameters.

In theory, $C_{int} = \gamma C_g$. From part a) and b), we would expect γ=2.57/1.97 = 1.30. This agrees well with the measured γ.

γ should be the most accurate of the values as it is extracted directly from delay measurements, using inverters that are driven and loaded by real inverters. The extraction of C_{int} should also be fairly good - C_{int} models the intrinsic capacitance as an ideal capacitor and the extraction lumps it together with ideal capacitance test loads.
The extraction of C_g is the least reliable, trying to characterize the wiggly input voltage curve with a single slope value, and driving the input with a constant current isn't very realistic of how the inverter behaves in actual use. Even so, the value extracted fits the other extracted values quite well, so as a practical matter, these nonidealities are not a big deal.

Problem #2 Inverter Sizing and Wire Delay

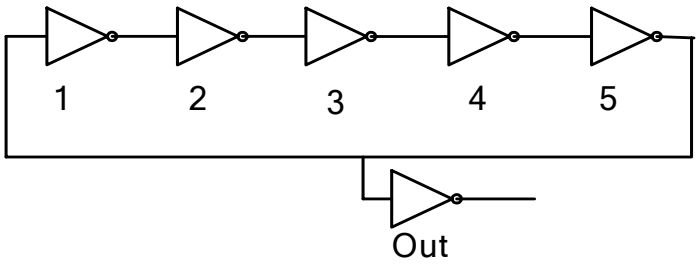


Figure 1

Figure 1 shows a ring oscillator with an output tap. Ring oscillators can be used in evaluating the gate delay in a certain technology (see pp. 28-29). We will use it in a slightly different way. Assume the intrinsic propagation delay of a minimum-size inverter is 30ps. Also assume the input capacitance is C_g=3fF and γ=2.

a) Calculate the frequency of oscillation of the ring oscillator built with minimum-size inverters. Note that inverter 5 has a different delay than 1 through due to extra loading from the output buffer. Assume the output buffer is also minimum-size.

Gates 1 through 4 are loaded with a fanout of 1, while gate 5 drives a fanout of 2. The total delay is thus:

$Tp = 4*tp_0(1+1/\gamma) + tp_0(1+2/\gamma)$
$= tp_0(5+6/\gamma) = 30ps*(5+6/2) = 240ps$

Note that the 5 and 6 correspond to the number of gates and the total fanout being driven by those gates. Starting from an instant when gate 5 drives gate 1 with a rising edge, this delay represents the time it takes for the edge to get through all the gates and

create a falling edge at the output of gate 5. Another Tp later, gate 5's output rises again – a total of 2Tp since the previous rising edge. The period of oscillation is thus 2*Tp, for a frequency of:

$f=1/(2Tp) = 1/(480ps) = 2.08GHz$

b) Find C_{int} and R_{eq} for an inverter.

$C_{int} = \gamma C_g = 2*3fF = 6fF$
$tp_0 = 0.69* R_{eq*} C_{int} \quad => R_{eq} = tp_0/(0.69*C_{int}) = 30ps/(0.69*6fF) = 7.25k\Omega$

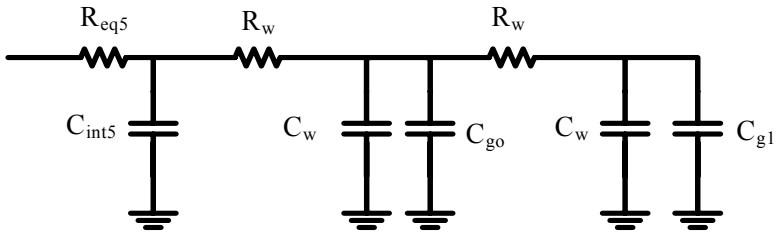
c) Now suppose that inverter 5 is connected to the output buffer with a metal-1 wire of width 1 μm and length 0.5mm, and that inverter 1 is connected to this point by an identical wire. Find the lumped-element resistance and capacitance of this wiring. Assume field oxide underneath the metal and no other wiring in the vicinity. Use Table 4.2 in Chapter 4 for capacitance values. The sheet resistance of aluminum in metal layers 1 through 4 is 0.075Ω/□.

$R_w = 0.5mm/1\ \mu m * 0.075\Omega/\square = 37.5\Omega$

Capacitance consists of two components – parallel plate, and fringe:

$C_{parallel\text{-}plate} = 0.5mm/1\mu m*30aF/\mu m^2 \quad = 15fF$
$C_{fringe} \quad = 2*0.\ 5mm*40aF/\mu m \quad = 40fF$
for a total of: $C_w = 55fF$

d) Sketch a schematic for an RC model of the connection between inverter 5, 1 and the output buffer, assuming each wire segment's capacitance to be at the end farthest away from inverter 5. Write an expression for the delay of inverter 5 driving inverter 1 (see Eq. 4.14 in the text), lumping together all terms that depend on the size of inverter 5.



$tp_5 \quad = 0.69\ (\ R_{eq5}C_{int5} + (R_{eq5}+R_w)(C_w+C_{go}) + (R_{eq5}+2*R_w)(\ C_w+C_{g1})\ )$
$\quad = 0.69\ R_{eq5}(C_{int5} + 2*C_w + C_{go} + C_{g1}) \ + \ 0.69\ R_w(3*C_w + C_{go} + 2*C_{g1})$

e) Find the oscillation frequency of the ring oscillator with these wiring parasitics.

Tp $= 4*tp_0(1+1/\gamma) + 0.69\ R_{eq5}(C_{int5} + 2*C_w + C_{go} + C_{g1}) + 0.69\ R_w(3*C_w + C_{go} + 2*C_{g1})$
$= 4*30ps(1+1/2) + 0.69 *7.25k\Omega(6 + 110 + 3 + 3\ fF) + 0.69* 37.5\Omega\ (3*55+3+6fF)$
$= 180ps + 610ps + 4.5ps = 794.5ps$

$f=1/(2Tp) = 1/(2*794.5ps) = 629MHz$

f) Keep inverter 1 and the output inverter at minimum size and size the other inverters to maximize the frequency of oscillation with the wiring present. What is the maximized frequency?

From the answer for part d, the part of the delay dependant on the size of inverter 5 is:

$0.69\ R_{eq5}(C_{int5} + 2*C_w + C_{go} + C_{g1})$

This is the delay of inverter 5 driving $2*C_w + C_{go} + C_{g1} = 116fF$. This is 38.66 times the unit gate capacitance of 3fF. We know from lecture 9 that the optimal tapering to drive this is a geometric taper with $f=38.66^{(1/5)} = 2.08$. Inverter 5 would be scaled to $2.08^4=18.6$ times minimum. The time for R_{eq5} to drive its load capacitance then looks the same as the other inverters in the chain driving their loads, so:

Tp $= 4*tp_0(1+2.08/2) + 0.69\ 7.25\ k\Omega/2.08^4*(\ 6*2.08^4 + 116\ fF\ ) + 0.69*\ 37.5\Omega\ *\ (3*55+3+6fF)$
$= 5*tp_0(1+2.08/2) + 0.69*\ 37.5\Omega\ (3*55+3+6fF)$
$= 5*30ps*2.04 + 4.5ps = 310ps$

$f=1/(2Tp) = 1/(2*310ps) = 1.61GHz$

g) Still keeping the output inverter at minimum size, and inverter 5 at the size just found, this time allowing inverter 1 to be resized along with the rest of the ring, can you increase the oscillation frequency further? If so, give the new fanout factor. You do not need to give the new oscillation frequency.

If we collect C_{g1} terms in the answer for part d), we have:

$tp_5 = 0.69\ (\ R_{eq5}C_{int5} + (R_{eq5}+R_w)(C_w + C_{go}) + (R_{eq5}+2*R_w)(\ C_w + C_{g1})\ )$
$= 0.69\ (\ R_{eq5}+2*R_w)C_{g1}\ +$ terms independent of C_{g1}
$= 0.69\ (7.25\ k\Omega/2.08^4 + 75\Omega)\ C_{g1} +$ other terms
$= 0.69\ (465\Omega)\ C_{g1} +$ other terms
$= 0.69\ (7.25\ k\Omega/15.6)C_{g1} +$ other terms

Thus the delay behaves as though inverter 1 were driven by an inverter 15.6 times minimum. The inverters scale geometrically between this factor (for a fictitious

inverter 0 driving inverter 1) and the 18.6 from before for inverter 5. The new fanout factor would be $(18.6/15.6)^{(1/5)} = 1.035$, or practically no taper. In essence, we've just scaled the entire chain larger to make the loading relatively smaller.

Bonus) Can you suggest simple changes to the wiring to increase oscillation frequency even more?

Running the wire in M2 or an even higher metal layer would reduce the capacitance of the wire. Also, so far, the wire resistance does not contribute significantly to the delay (although it would with further scaling of the inverters) so reducing the width of the wires can also help to reduce the parallel-plate component of the wiring capacitance. This improvement would be marginal however, as the capacitance is mostly fringing capacitance that does not go away.

If we continued with iterating parts f) and g) to further reduce delay, we will get to a point where the wiring resistance becomes significant and increasing the wire width can also help, by reducing this resistance. Although the parallel plate capacitance increases by the same factor as the reduction in resistance, the total capacitance will increase by a smaller factor as long as fringing capacitance is a significant part of the total.